REMARKS

I. Status of Claims

Claims 1-6 are pending.

II. April 2002 Disclosure Document Enclosed

The April 2002 Disclosure Document referenced in the Affidavit under 37 CFR §1.131 submitted in the prior response dated October 2, 2006 was inadvertently omitted from that response. The April 2002 Disclosure Document is enclosed herein to remedy the omission.

Applicants incorporate herein the arguments made in the October 2, 2006 response that they conceived of the invention and reduced it to practice more than one year before Beraudo was published. The affidavit establishes facts showing invention and the reduction of practice before June 2005. Therefore, Applicants respectfully argue that Beraudo cannot be used as prior art under Section §102(e), (a), or (b) and Applicants respectfully request that this rejection be withdrawn.

III. Claim Rejection Under 35 USC §102 (b)

The Examiner has rejected claims 1-6 under 35 USC 102(b) as being anticipated by an article dated November 1996 by Togawa et al. ("Togawa"). A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers, Inc. v. Union Oil Co. of California*, 2 USPQ2nd 1051 at 1053 (Fed. Cir. 1987).

A. Togawa Does Not Disclose Each and Every Element

Togawa is directed to a multi-FPGA circuit. Togawa repeatedly asserts that the invention is specifically for logic circuits with multiple FPGA chips by using the phrase "multi-FPGA." See, e.g., the title of Togawa "...for Multi-FPGA Systems"; Section 1; Section 2.3. Figures 1 and 2 show multiple FPGA's. Tables 2-5 show circuit partitions for 2,4,6,8 and 16 FPGA chips. Further, the formulas for implementing the invention disclosed for Togawa use variables referencing more

than one chip, such as c_1 and c_2, as well as *D*, the interchip routing delay. Togawa focuses its discussion on the delay of interconnecting two chips and minimizing the number of nets crossing between chips. See, e.g. Section 3.3. Clearly, Togawa is directed to improving performance of the logic of a multi-chip system and not for improving performance of a single FPGA.

Conversely, Applicants claim a method for optimizing performance within a single FPGA. See claims 1 and 5 which claim and repeatedly refer to a single FPGA with the phrase "...in an FPGA..." Because Togawa is directed to the delay between chips in a multi-chip system, it does not disclose an invention for use on a single FPGA. Therefore, Togawa does not expressly or inherently disclose one of the elements of Applicants' claimed invention and cannot anticipate it. Applicants respectfully request that this rejection be withdrawn.

B. Togawa Would Not Work on a Single FPGA

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers, Inc.* Under the principles of inherency, if the prior art in its normal and usual operation would necessarily perform the method claimed, then the method claimed will be considered to be anticipated. MPEP §2112.02. *See MEHL/Biophile Int'l Corp. v. Milgraum*, 52 USPQ2d 1303, 1305 (Fed. Cir. 1999), citing *In re King*, 231 USPQ 136, 138 (Fed. Cir. 1986)) However, the fact that a certain result or characteristic *may* occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. MPEP §2112.02 citing *In re Rijckaert, 28 USPQ2nd 1955, 1957 (Fed. Cir. 1993). In re Oelrich and Divigard, 212 USPQ 323,326, citing Hansgird v. Kemmer, 40 USPQ 665.*

Togawa's invention would not work on a single FPGA in its normal and usual operation because Togawa's solution minimizes the delays in a chosen critical path by reducing the number crossings between the chips, which reduces delay, but does not apply to reduction of the delays for a critical path inside a chip. The sources of the delays between chips are different from those within a chip, and therefore require different solutions. The Togawa solutions cannot be implemented

on a single chip because a single chip does not have the same physical connections. Togawa notes that in applying the suggested partitioning algorithm that path delays between circuit elements are ignored except during the selection of the critical to be optimized. This is in contrast to the subject invention which minimizes path delays through the duplication of logic within a single chip. Therefore, Togawa does not inherently disclose a solution for improving the performance of a single chip because it cannot be implemented on a single chip.

Togawa does not expressly or inherently disclose one of the elements of Applicants' claimed invention and cannot anticipate it. Applicants respectfully request that this rejection be withdrawn.

CONCLUSION

Applicants respectfully submit that all objections and rejections have been traversed, and that the application is in form for issuance.

Respectfully submitted,

4/3/07

Dated

Sandra L. Etherton
Registration No. 36,982
Tel: 602-681-3331

Russell W. Guenthner
Registration No. 54,140
Tel: 602-862-5479

Bull HN Information Systems Inc.
MS B55
13430 North Black Canyon Highway
Phoenix, AZ 85029

Bull HN Information Disclosure Document

BULL HN INFORMATION SYSTEMS INC.
INVENTION DISCLOSURE - Rev. April 8, 2002 -

Bull

Please complete this form promptly and submit it to the Bull HN Law Office. Please do not delay; missing or incomplete information can be supplied later. ("*" items are optional)	**FOR LAW OFFICE USE:** Docket Number: 5200 3218 Attorney/Agent:

1. Proposed **descriptive working title** for the invention: (should be short and technically correct)

METHOD FOR IMPROVING PERFORMANCE OF CRITICAL PATH IN FIELD PROGRAMMABLE GATE ARRAYS

2. Date: April 12, 2002 3. Conception Date: September 2001

3. When will (or was) the invention first functional, or when will it be known to be completely conceptually feasible (reduced to practice) ?

January, 2002

4. In what Bull product(s), if any, is it used or to be used? (specify dates):

Olympus 2

5. People who participated in the invention:
(Include all those who contributed to the invention)

Russell W. Guenthner, David W. Selway, Clint B. Eckard, Charles Ryan, Eric Conway

6. Very brief summary of the invention:

A methodology for improving the timing of specific critical paths in an Field Programmable Gate Array (FPGA) implementation of a logic circuit without significantly affecting the timing of other logic paths. The method utilizes logic replication and specific guidelines for placement of the logic gates involved in a critical path to optimize the timing of that critical path. The logic gates involved in a critical path are replicated and placed or simply moved such to implement the desired logic with nearly the shortest total distance for routing of signals involved in the critical path. The optimization can be done with small impact on the timing of other paths because of certain characteristics of routed signals in specific Field Programmable Gate Arrays such as those in the Virtex family of FPGAs from Xilinx Corporation. The interconnect technology from Xilinx that has this characteristic has been named by named by Xilinx as "Active Interconnect Technology".

7. Field(s) of the Invention: *
(related subjects or words that might classify the invention)

Field Programmable Gate Arrays (FPGAs), and methodology for improving the performance of logic that appears as a critical timing path. Logic design, logic synthesis, gate array placement algorithms, duplication of logic for improved performance, and iterative approaches for improvement of the implementation and timing of a logic function within an integrated circuit chip, a gate array chip, or a field programmable gate array.

8. Related Patents: *

not yet searched

9. Description of the invention: (starting on a separate page)

(This is a guideline for what is needed. Do not delay if everything is not available or complete).

a. Describe the problem being solved.
b. Provide a description of the prior art, including sketches if that is helpful. That is, describe how the problem was previously solved, or how was it done before this new invention.
c. Describe the features of the invention, including what is new, unique or advantageous about the invention when compared to the prior art.
d. Include sketches or drawings that are useful to understand the invention. Include flow charts, especially for software inventions.
e. Include reference documentation to assist in understanding the invention, or provide a list of reference material.
f. Clearly list the essential elements of the invention.

The present invention provides a method for optimizing the timing of a specific logic path with more rapid convergence on a solution of overall goodness than methodology of the prior art. The invention is based upon observation of the routing and delay characteristics for Field Programmable Gate Arrays (FPGAs) in the Virtex family of FPGA devices manufactured by the Xilinx corporation.

In most implementations of electronic circuits the logic delay from one circuit that is the source of a signal to those circuits which are loads on the signal can be roughly characterized as a function which increases with both additional loads and also with additional distance between the source and the loads. Oftentimes the delay function is complicated by issues such as signal reflection but those experienced in the art will recognize that in general adding either load or distance (or both) is likely to increases delay. For this reason, methods for optimizing the overall goodness of a circuit design will typically try to minimize both loading and distance. Typically, loading is minimized by a method of logic synthesis followed by logic optimization. Typically, distance is minimized by a method which tries to place individual gates which implement the synthesized circuits such that both the length of individual nets and also the overall total length of all nets is minimized.

There are many methods of logic circuit synthesis, logic optimization, and logic placement which attempt to minimize gate count, logic net distance and overall circuit delay such that the overall goodness of a circuit is maximized. Using these methods sometimes results in a design for which a solution is not readily apparent or for which the computer algorithms which choose and evaluate potential solutions do not converge on a solution which meets all of the requirements. This failure to find a solution often happens because changing the implementation of logic to improve one critical timing path may adversely impact the timing of another path either by changing the loading of signals in the other path, or by adversely affecting the placement of circuits involved in the other path. The detrimental effects can be either caused directly by moving or changing circuits in both paths or indirectly by logic changes which impact the other circuit by forcing such things as a change in placement or a change in the routing of signals that pass through the same areas of logic. These effects are often difficult to analyze or predict.

In the Virtex family of FPGAs from Xilinx it has been observed that these devices have a somewhat unique delay characteristic which assumedly is due to the nature of the circuit implementation inside the Xilinx FPGAs. The characteristic of delay related to this invention is that the signal delay from a given source to a given load is mostly independent of other loads which are also found on the net. That is, for a net which connects a source gate to multiple loads, the delay function for any given load is a function mainly of the distance from the source to that load and the effect of other loads on that delay is small, including the effect of both the electrical loading and the electrical distance involved. The observation of this characteristic allows for an improved method of logic optimization. The implementation for interconnect on the Xilinx Virtex devices for which this characteristic has been observed has been described as follows by Xilinx:

"Xilinx Active Interconnect technology, built on the strength of the fourth generation segmented routing technology, provides full buffering at each routing interconnect point. This eliminates the variable routing delay effects of conventional interconnect architectures, where the total routing delay depends on the fan-out. With the conventional interconnect architecture, the routing delay of a particular node may be changed during design iteration, which makes complex designs like the ten million-system gates design impractical. In contrast, Active Interconnect technology allows precise delay calculations that are generally independent of signal fan-out."

After a logic design has been implemented on an FPGA through any process of logic synthesis, logic optimization and logic placement an analysis of the timing characteristics can be performed and the results analyzed to identify critical timing paths which need further change or optimization of some kind to improve the timing of those paths. It can often be observed that the placement of logic involved in any one specific path could be improved, but the effect of moving logic to improve that path may prove detrimental to the timing of other logic paths. The characteristic of the Xilinx Virtex FPGA which minimizes interdependencies between multiple loads on a source gate allows for an optimization of a specific path to be proposed which has minimal effect on other logic paths. This relatively easy to analyze improvement can be applied to only those paths which are most critical with respect to timing and because the changes have little impact on the timing of other paths it is more likely that the changes will

achieve overall success. More specifically, the changes to improve one path will not be much to the detriment of other paths so progress towards achieving overall good timing can be made.

The specific method for making these final improvements in logic implementation and logic placement is to take a critical path and implement it in a relatively straight line physical path with logic duplicated or moved as needed to achieve optimal implementation of that path. Any logic which is involved with other critical paths is replicated; any logic which is involved in only this specific critical path is simply moved. The only restriction on the logic implementation is that it must be fit into the existing layout of the circuit without too much effect on the placement of other logic. Since the Virtex chip provides interconnect and routing of signals from a source to a specific load in a manner such that the timing characteristic for that load that has been observed to be relatively independent of other loads, then the implementation of any one critical path can be implemented with logic physically place in as straight a line as possible and with optimal logic implementation without having too much detrimental effect on other logic paths. There are limits on the number of paths to which this broad optimization can be applied since it is likely that the amount of logic required for the optimal implementation with respect to timing will be larger than originally proposed implementation.

A specific embodiment of the invention would be a method in which logic implementation and placement is done in any conventional manner. This is followed by identification of the critical timing paths with the logic involved on a critical path depicted on a floorplan. The interconnect of the logic gates in this path are then observed. Any logic gate that is a source for signals involved in another critical path is replicated and then placed as close as possible to a location in a straight line along the desired physical path. Any logic gate which is not connected to other critical paths is simply moved to a more desirable location, that is, a location as near as possible to an implementation lying on a straight line from the beginning of the logic path to the end.

DRAWINGS